REMARKS

Claims 1-4, 6, 8-12, 14, 16-18, and 20-24 are pending in the Application. Claims 1, 9, and 17 are independent claims. Claims 1, 9, and 17 have been amended. Claims 5, 7, 13, 15, and 19 have been canceled.

Claim Rejections - 35 USC § 103(a)

The Patent Office rejected Claims 1-5, 7-13, 15-17 and 24 under 35 U.S.C. § 103(a) as being unpatentable over Voogel et al. (U.S. Patent No. 6,362,651) ("Voogel") in view of Muthujumaraswathy et al. (U.S. Patent No. 6,279,045) ("Muthujumaraswathy"). The Patent Office also rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Muthujumaraswathy further in view of Mastro et al. (U.S. Publication No. 2002/0091977) ("Mastro"). The Patent Office also rejected Claims 18 and 20-23 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Muthujumaraswathy further in view of Lee et al. (U.S. Patent No. 6,222,212) ("Lee"). The Patent Office also rejected Claim 19 under 35 U.S.C. § 103(a) as being unpatentable over Voogel in view of Muthujumaraswathy further in view of Hung et al. (U.S. Patent No. 6,396,129) ("Hung").

Applicant respectfully traverses the rejections. "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." MPEP § 2142. In order to establish a prima facie case, the examiner must ascertain the differences between the claim and the prior art. MPEP § 2141. "All words in a claim must be considered in judging the patentability of that claim against the prior art." MPEP § 2143.03, citing *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03, citing *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Applicant respectfully submits Claims 1-4, 6, 8-12, 14, 16-18, and 20-24 include elements that are not disclosed by the available prior art. For example, Claim 1 recites:

> A method for providing field programmable platform array units, comprising:
> cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units,...
> wherein said single platform array unit platform is a digital signal processing (DSP) platform.

Voogle and Muthujumaraswathy, alone or in combination, do not disclose the above limitations. The Patent Office cites to Muthujumaraswathy for disclosing the single platform array unit platform is a digital signal processing (DSP) platform, stating that "said single platform is a digital signal processing (DSP) platform (Muthujumaraswathy, col. 3, line 62 note: a processor)" (February 4, 2009 Office Action, p. 5). However, Applicant respectfully disagrees with this interpretation of Muthujumaraswathy. The cited portion of Muthujumaraswathy comes from of a portion of text used to list the meaning of common acronyms (col. 3, line 50 through col. 4, line 49), disclosing "The following terms, abbreviations and acronyms may be used in the description contained herein." There is no other reference to a DSP in Muthujumaraswathy. Thus, Muthujumaraswathy discloses the term DSP is an acronym for digital signal processor. Disclosing an acronym is not equivalent to disclosing **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.*

The disclosure of Voogel does not cure the defects of Muthujumaraswathy. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within *a single platform array unit platform...wherein*

said single platform array unit platform is a digital signal processing (DSP) platform. Neither Voogel nor Muthujumaraswathy disclose a platform array unit platform is a DSP platform. Voogel and Muthujumaraswathy, alone or in combination, do not disclose **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.* Claim 1 is believed allowable for at least the above reasons.

Further, Claim 1 also recites:

> A method for providing field programmable platform array units, comprising: cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units,...
> wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.

Voogle, Muthujumaraswathy, and Hung, alone or in combination, do not disclose the above limitations. The Patent Office cites to Hung for disclosing encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal, stating that "Huang(sic) discloses encapsulation 150 of lower copper layer (Fig. 3C, col. 4, lines 20-43)" (February 4, 2009 Office Action, p. 7). The cited portions of Hung are reproduced below:

> As shown, during package assembly process, a silver epoxy layer 150 is pasted over the die-mounting area 111 of the die pad 110 to a thickness that can cover the dot array of silver-plated regions 141. Next, a semiconductor chip 160 (which has an active surface *160a* and an inactive surface *160b)* has its inactive surface *160b* adhered by means of the silver-epoxy layer 150 to the die-mounting area 111 of the die pad 110. After this, a wire-bonding process is performed to bond a plurality of bonding wires 170, including a set of I/O wires 171 bonded from the active surface *160a* of the semiconductor chip 160 to the inner-lead portion 120 of the leadframe 100 and at least one ground wire 172 down bonded from the active *surface 160a of* the semiconductor chip 160 to the silver-plated peripheral area 142 on the ground-wire bonding area 112 of the die pad 110. Finally, a molding process is performed to form an encapsulation body 180 to encapsulates the semiconductor chip 160 together with the inner-lead portion 120, the silver-epoxy layer 150, the bonding wires 170, and the front side *110a* of the die pad 110, while exposing the back side *110b* of the die pad 110 to the outside.

As shown above, Hung discloses "a molding process is performed to form an encapsulation body 180 to encapsulates(sic) the semiconductor chip 160 together with the inner lead portion 120..." Thus Hung discloses a standard plastic package encapsulating process of a semiconductor. A standard plastic package encapsulating process of a semiconductor is not equivalent to **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.***" However, Applicant respectfully disagrees with this interpretation of Muthujumaraswathy. The cited portion of Muthujumaraswathy comes from of a portion of text used to list the meaning of common acronyms (col. 3, line 50 through col. 4, line 49), disclosing "The following terms, abbreviations and acronyms may be used in the description contained herein." There is no other reference to a DSP in Muthujumaraswathy. Thus, Muthujumaraswathy discloses the term DSP is an acronym for digital signal processor. Disclosing an acronym is not equivalent to disclosing **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.*

The disclosures of Voogel and Muthujumaraswathy do not cure the defects of Hung. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.*** Muthujumaraswathy discloses a chip including a processor core and a block of user-programmable logic. A chip including a processor core and a block of user-programmable logic is not equivalent to **a method for providing field programmable platform**

array units, comprising: cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.***

Hung does not disclose a standard die seal. Neither Voogel nor Muthujumaraswathy disclose a standard die seal. Voogel, Hung, and Muthujumaraswathy, alone or in combination, do not disclose **a method for providing field programmable platform array units**, comprising: cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.*** Claim 1 is believed allowable for at least the above reasons.

Claims 2-4, 6, and 8 depend upon Claim 1 either directly or indirectly and are allowable under *In re Fine* based on their dependence upon allowable base claims.

Similarly, Claim 9 recites:

> A system for providing field programmable platform array units, comprising:
> means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer...
> wherein said single platform array unit platform is a digital signal processing (DSP) platform.

Voogle and Muthujumaraswathy, alone or in combination, do not disclose the above limitations. The Patent Office cites to Muthujumaraswathy for disclosing the single platform array unit platform is a digital signal processing (DSP) platform, stating that "said single platform is a digital signal processing (DSP) platform (Muthujumaraswathy, col. 3, line 62 note: a processor)" (February 4, 2009 Office Action, p. 5). However, Applicant respectfully disagrees with this interpretation of Muthujumaraswathy. The cited portion of Muthujumaraswathy comes from of a portion of text used to list the meaning of common acronyms (col. 3, line 50 through col. 4, line 49), disclosing "The following terms, abbreviations and acronyms may be used in the description contained herein." There is no other reference to a DSP in

Muthujumaraswathy. Thus, Muthujumaraswathy discloses the term DSP is an acronym for digital signal processor. Disclosing an acronym is not equivalent to disclosing **a system for providing field programmable platform array units,** comprising: means for cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.*

The disclosure of Voogel does not cure the defects of Muthujumaraswathy. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a system for providing field programmable platform array units,** comprising: means for cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.* Neither Voogel nor Muthujumaraswathy disclose a platform array unit platform is a DSP platform. Voogel and Muthujumaraswathy, alone or in combination, do not disclose **a system for providing field programmable platform array units,** comprising: means for cutting N by M array of platform array units within *a single platform array unit platform...wherein said single platform array unit platform is a digital signal processing (DSP) platform.* Claim 9 is believed allowable for at least the above reasons.

Further, Claim 9 also recites:

> A system for providing field programmable platform array units, comprising:
> means for cutting N by M array of platform array units within a single platform array unit platform from a field programmable platform array wafer according to an order for a customer, N and M being positive integers, said field programmable platform array wafer having all silicon layers and metal layers already built and including a plurality of platform array units,...
> wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.

Voogle, Muthujumaraswathy, and Hung, alone or in combination, do not disclose the above limitations. The Patent Office cites to Hung for disclosing encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal, stating that "Huang(sic) discloses

encapsulation 150 of lower copper layer (Fig. 3C, col. 4, lines 20-43)" (February 4, 2009 Office Action, p. 7). The cited portions of Hung are reproduced below:

> As shown, during package assembly process, a silver epoxy layer 150 is pasted over the die-mounting area 111 of the die pad 110 to a thickness that can cover the dot array of silver-plated regions 141. Next, a semiconductor chip 160 (which has an active surface *160a* and an inactive surface *160b)* has its inactive surface *160b* adhered by means of the silver-epoxy layer 150 to the die-mounting area 111 of the die pad 110. After this, a wire-bonding process is performed to bond a plurality of bonding wires 170, including a set of I/O wires 171 bonded from the active surface *160a* of the semiconductor chip 160 to the inner-lead portion 120 of the leadframe 100 and at least one ground wire 172 down bonded from the active *surface 160a of* the semiconductor chip 160 to the silver-plated peripheral area 142 on the ground-wire bonding area 112 of the die pad 110. Finally, a molding process is performed to form an encapsulation body 180 to encapsulates the semiconductor chip 160 together with the inner-lead portion 120, the silver-epoxy layer 150, the bonding wires 170, and the front side *110a* of the die pad 110, while exposing the back side *110b* of the die pad 110 to the outside.

As shown above, Hung discloses "a molding process is performed to form an encapsulation body 180 to encapsulates(sic) the semiconductor chip 160 together with the inner lead portion 120..." Thus Hung discloses a standard plastic package encapsulating process of a semiconductor. A standard plastic package encapsulating process of a semiconductor is not equivalent to **a system for providing field programmable platform array units**, comprising: means for cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.***

The disclosures of Voogel and Muthujumaraswathy do not cure the defects of Hung. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a system for providing field programmable platform array units**, comprising: means for cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.***

Muthujumaraswathy discloses a chip including a processor core and a block of user-programmable logic. A chip including a processor core and a block of user-programmable logic is not equivalent to **a system for providing field programmable platform array units**, comprising: means for cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.***

Hung does not disclose a standard die seal. Neither Voogel nor Muthujumaraswathy disclose a standard die seal. Voogel, Hung, and Muthujumaraswathy, alone or in combination, do not disclose **a system for providing field programmable platform array units**, comprising: means for cutting N by M array of platform array units within a single platform array unit platform...***wherein encapsulation of lower copper metal layers of said single platform array unit platform is preserved by a standard die seal.*** Claim 9 is believed allowable for at least the above reasons.

Claims 10-12, 14, and 16 depend upon Claim 9 either directly or indirectly and are allowable under *In re Fine* based on their dependence upon allowable base claims.

Similarly, Claim 17 recites:

> A semiconductor device, comprising:
> a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor;
> wherein interconnect between said plurality of platform array units being pre-routed;
> wherein said single platform array unit platform is a digital signal processing (DSP) platform;
> wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.

Voogle and Muthujumaraswathy, alone or in combination, do not disclose the above limitations. The Patent Office cites to Muthujumaraswathy for disclosing the single platform array unit platform is a digital signal processing (DSP) platform, stating that "said single platform is a digital signal processing (DSP) platform (Muthujumaraswathy, col. 3, line 62 note: a processor)" (February 4,

2009 Office Action, p. 5). However, Applicant respectfully disagrees with this interpretation of Muthujumaraswathy. The cited portion of Muthujumaraswathy comes from of a portion of text used to list the meaning of common acronyms (col. 3, line 50 through col. 4, line 49), disclosing "The following terms, abbreviations and acronyms may be used in the description contained herein." There is no other reference to a DSP in Muthujumaraswathy. Thus, Muthujumaraswathy discloses the term DSP is an acronym for digital signal processor. Disclosing an acronym is not equivalent to disclosing **a semiconductor device, comprising:** a plurality of platform array units within ***a single platform array unit platform***...wherein ***said single platform array unit platform is a digital signal processing (DSP) platform.***

The disclosure of Voogel does not cure the defects of Muthujumaraswathy. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a semiconductor device, comprising:** a plurality of platform array units within ***a single platform array unit platform***...wherein ***said single platform array unit platform is a digital signal processing (DSP) platform***. Neither Voogel nor Muthujumaraswathy disclose a platform array unit platform is a DSP platform. Voogel and Muthujumaraswathy, alone or in combination, do not disclose **a semiconductor device, comprising:** a plurality of platform array units within ***a single platform array unit platform***...wherein ***said single platform array unit platform is a digital signal processing (DSP) platform***. Claim 17 is believed allowable for at least the above reasons.

Further, Claim 17 also recites:

> A semiconductor device, comprising:
> a plurality of platform array units within a single platform array unit platform having portions being field programmable by a customer, each of said plurality of platform array units including at least one core and at least one pre-manufactured processor;
> wherein interconnect between said plurality of platform array units being pre-routed;
> wherein said single platform array unit platform is a digital signal processing (DSP) platform;

> wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.

Voogle, Muthujumaraswathy, and Hung, alone or in combination, do not disclose the above limitations. The Patent Office cites to Hung for disclosing encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal, stating that "Huang(sic) discloses encapsulation 150 of lower copper layer (Fig. 3C, col. 4, lines 20-43)" (February 4, 2009 Office Action, p. 7). The cited portions of Hung are reproduced below:

> As shown, during package assembly process, a silver epoxy layer 150 is pasted over the die-mounting area 111 of the die pad 110 to a thickness that can cover the dot array of silver-plated regions 141. Next, a semiconductor chip 160 (which has an active surface *160a* and an inactive surface *160b)* has its inactive surface *160b* adhered by means of the silver-epoxy layer 150 to the die-mounting area 111 of the die pad 110. After this, a wire-bonding process is performed to bond a plurality of bonding wires 170, including a set of I/O wires 171 bonded from the active surface *160a* of the semiconductor chip 160 to the inner-lead portion 120 of the leadframe 100 and at least one ground wire 172 down bonded from the active *surface 160a of* the semiconductor chip 160 to the silver-plated peripheral area 142 on the ground-wire bonding area 112 of the die pad 110. Finally, a molding process is performed to form an encapsulation body 180 to encapsulates the semiconductor chip 160 together with the inner-lead portion 120, the silver-epoxy layer 150, the bonding wires 170, and the front side *110a* of the die pad 110, while exposing the back side *110b* of the die pad 110 to the outside.

As shown above, Hung discloses "a molding process is performed to form an encapsulation body 180 to encapsulates(sic) the semiconductor chip 160 together with the inner lead portion 120..." Thus Hung discloses a standard plastic package encapsulating process of a semiconductor. A standard plastic package encapsulating process of a semiconductor is not equivalent to **a semiconductor device...wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.**

The disclosures of Voogel and Muthujumaraswathy do not cure the defects of Hung. Voogel discloses a method for producing multi-device PLDs by dicing a wafer into multi-chip PLDs. Producing multi-device PLDs by dicing a wafer into multi-chip PLDs is not equivalent to **a semiconductor device...wherein encapsulation of lower copper metal layers of said**

semiconductor device is preserved by a standard die seal. Muthujumaraswathy discloses a chip including a processor core and a block of user-programmable logic. A chip including a processor core and a block of user-programmable logic is not equivalent to **a semiconductor device...wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.**

Hunge does not disclose a standard die seal. Neither Voogel nor Muthujumaraswathy disclose a standard die seal. Voogel, Hung, and Muthujumaraswathy, alone or in combination, do not disclose **a semiconductor device...wherein encapsulation of lower copper metal layers of said semiconductor device is preserved by a standard die seal.** Claim 17 is believed allowable for at least the above reasons.

Claims 18 and 20-24 depend upon Claim 17 either directly or indirectly and are allowable under *In re Fine* based on their dependence upon allowable base claims.

The Patent Office rejected Claims 6 and 14 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Muthujumaraswathy in further view of Mastro. Applicant respectfully traverses. Claim 6 depends from Claim 1, which is allowable for the reasons stated above, and is believed allowable under *In re Fine* based on its dependence upon an allowable base claim. Claim 14 depends from Claim 9, which is allowable for the reasons stated above, and is thus believed allowable under *In re Fine* due to its dependence upon an allowable base claim.

The Patent Office rejected Claims 18 and 20-23 under 35 U.S.C. § 103(a) as being unpatentable over Voogel and Shigeki in view of Lee. Applicant respectfully traverses. Claims 18 and 20-23 depend from Claim 17, which is allowable for the reasons stated above, and are believed allowable under *In re Fine* due to their dependence on an allowable base claim.

CONCLUSION

In light of the forgoing, reconsideration and allowance of the claims is earnestly solicited.

Respectfully submitted,
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